

FIG. 1A

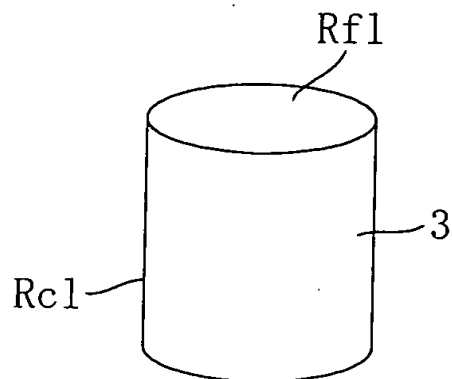


FIG. 1B

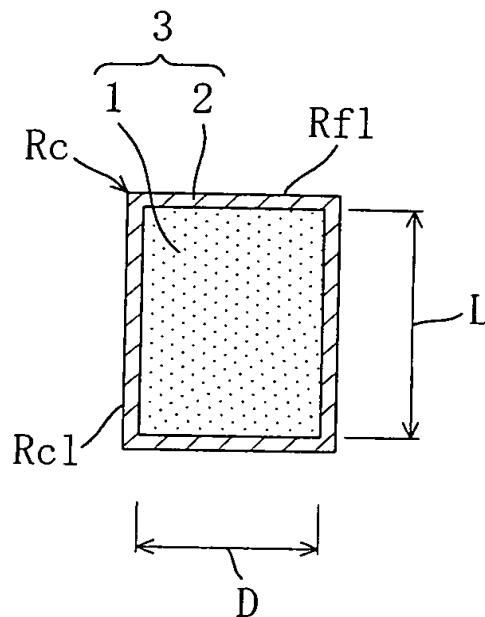
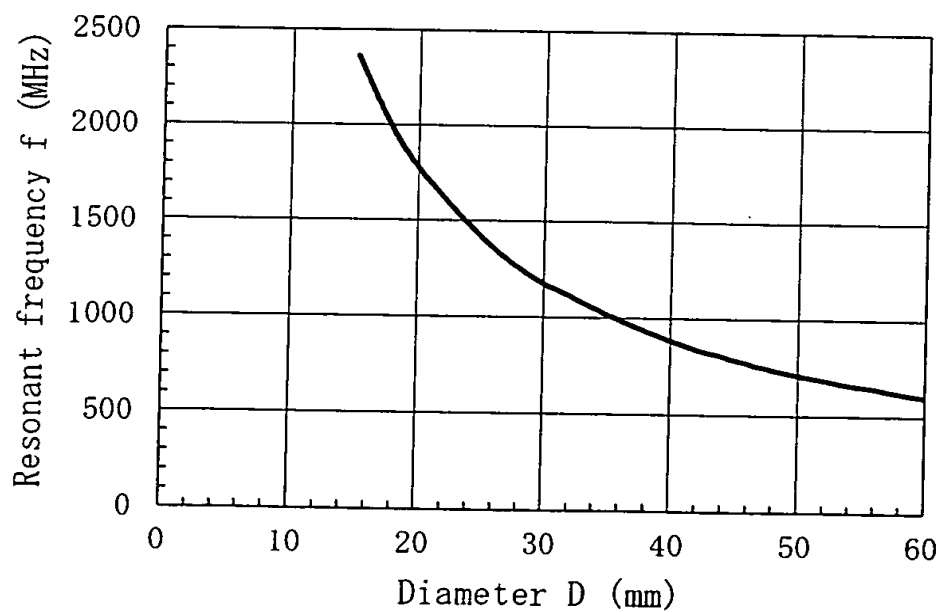


FIG. 2



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FIG. 3

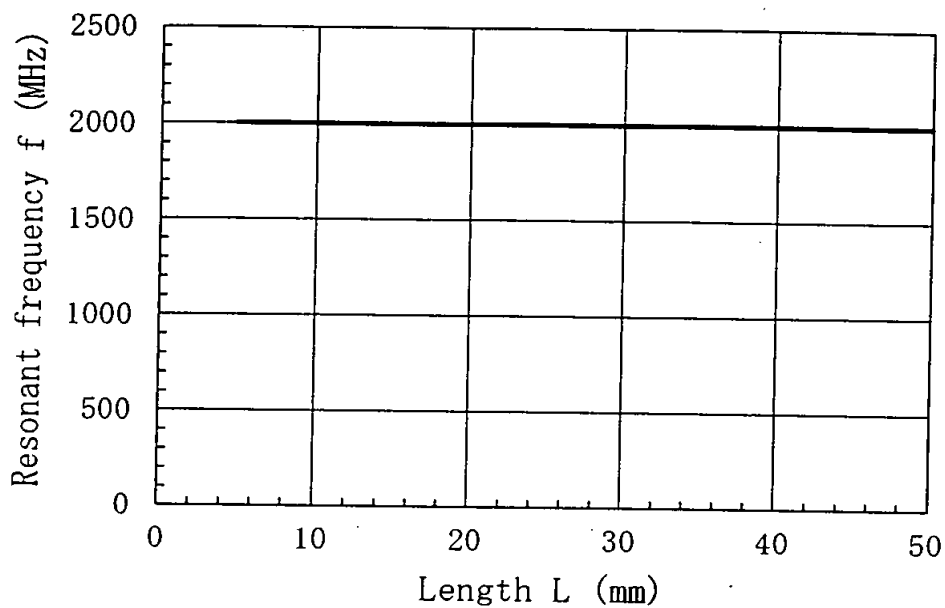
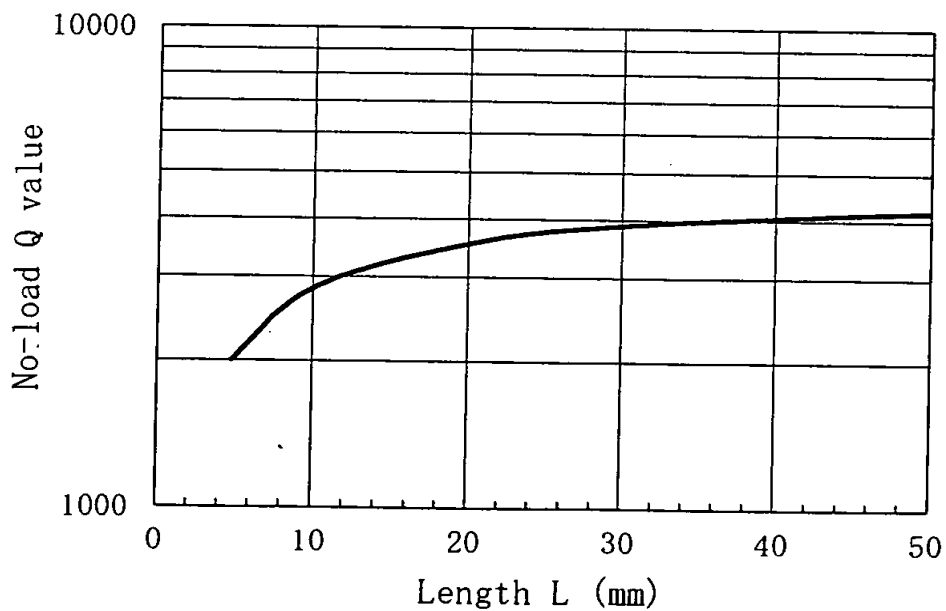


FIG. 4



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FIG. 5

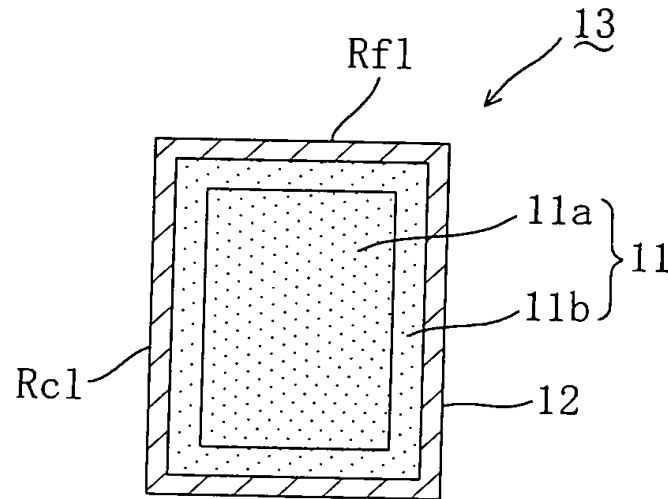
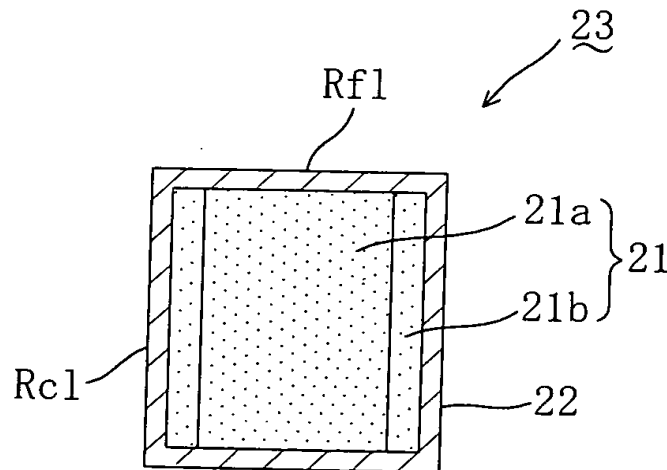


FIG. 6



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FIG. 7

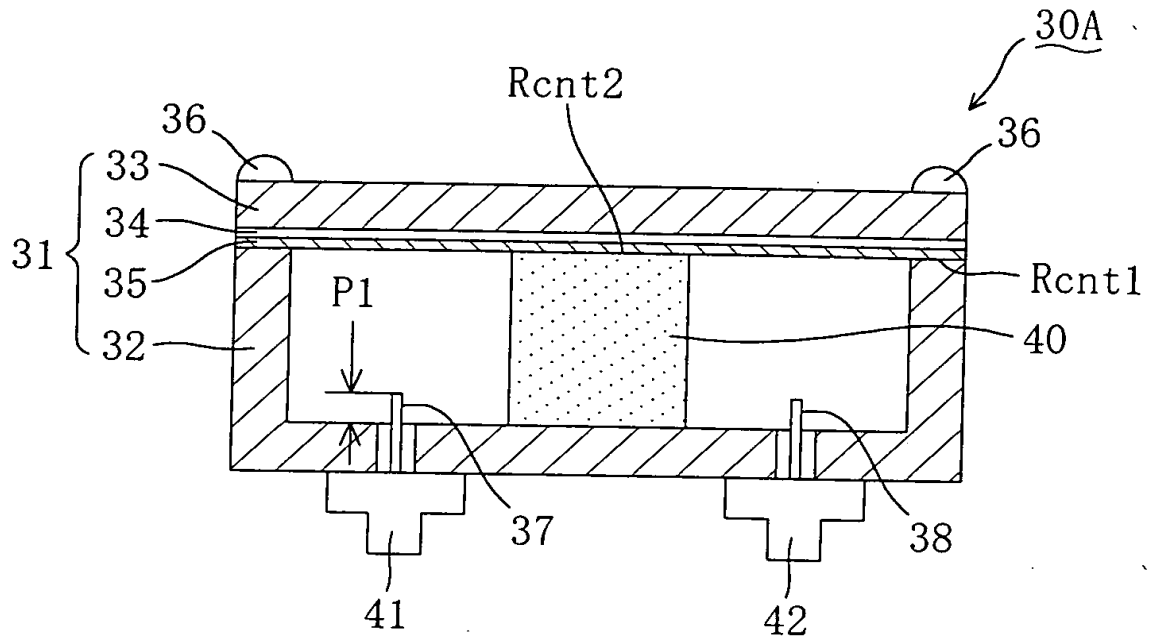
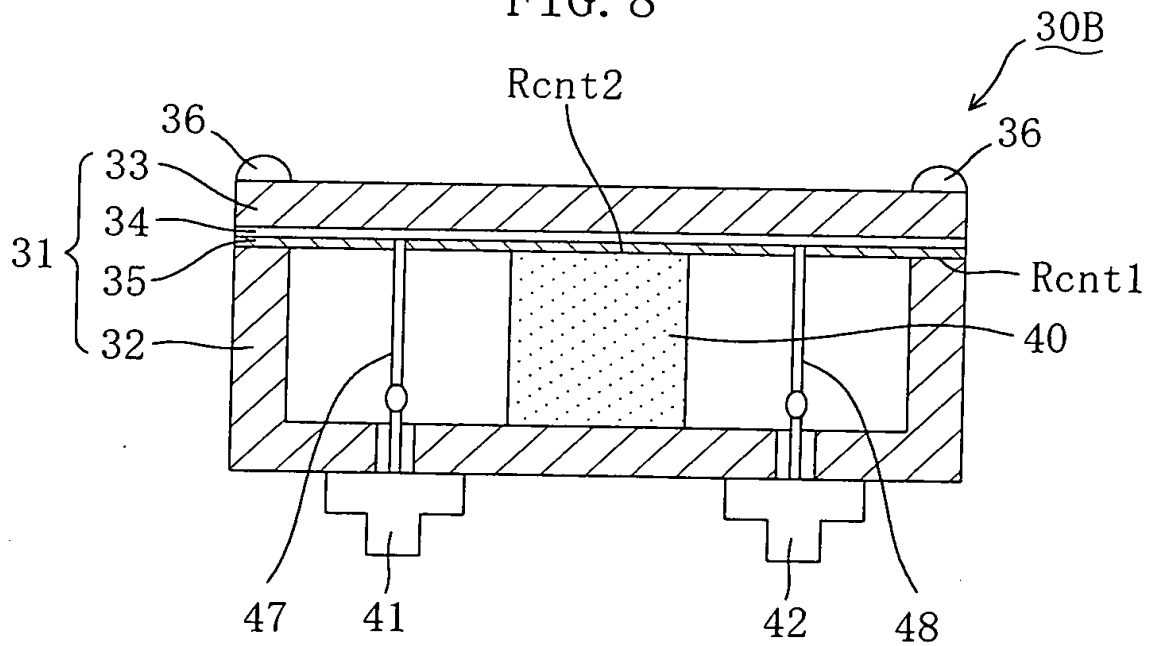


FIG. 8



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FIG. 9

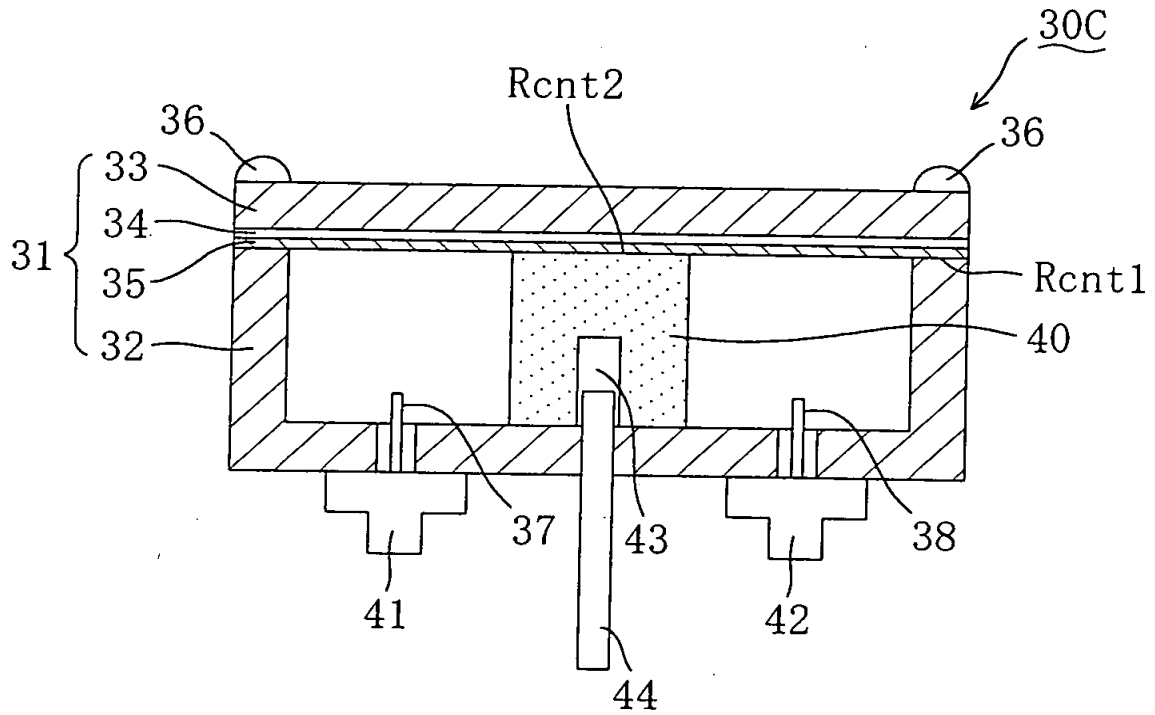


FIG. 10

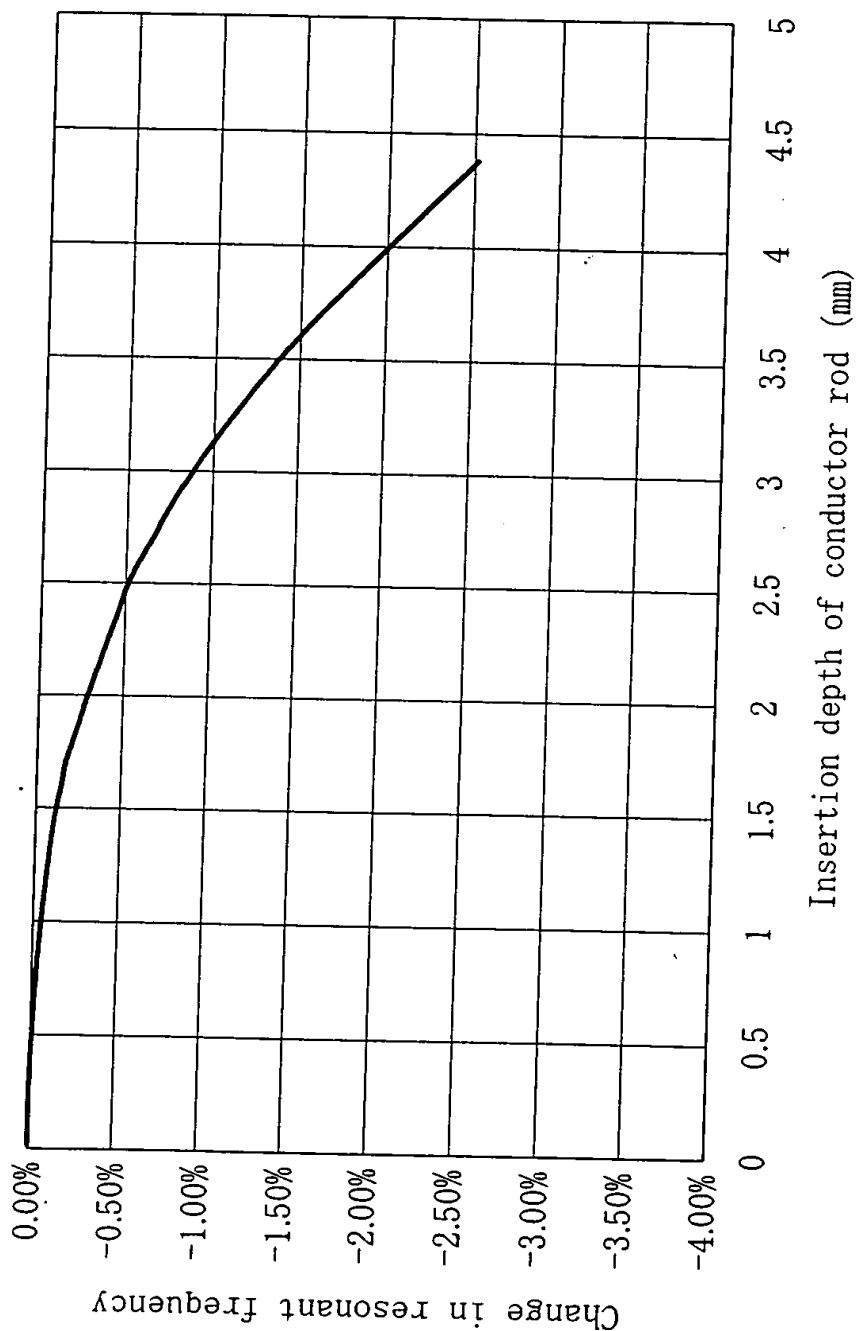
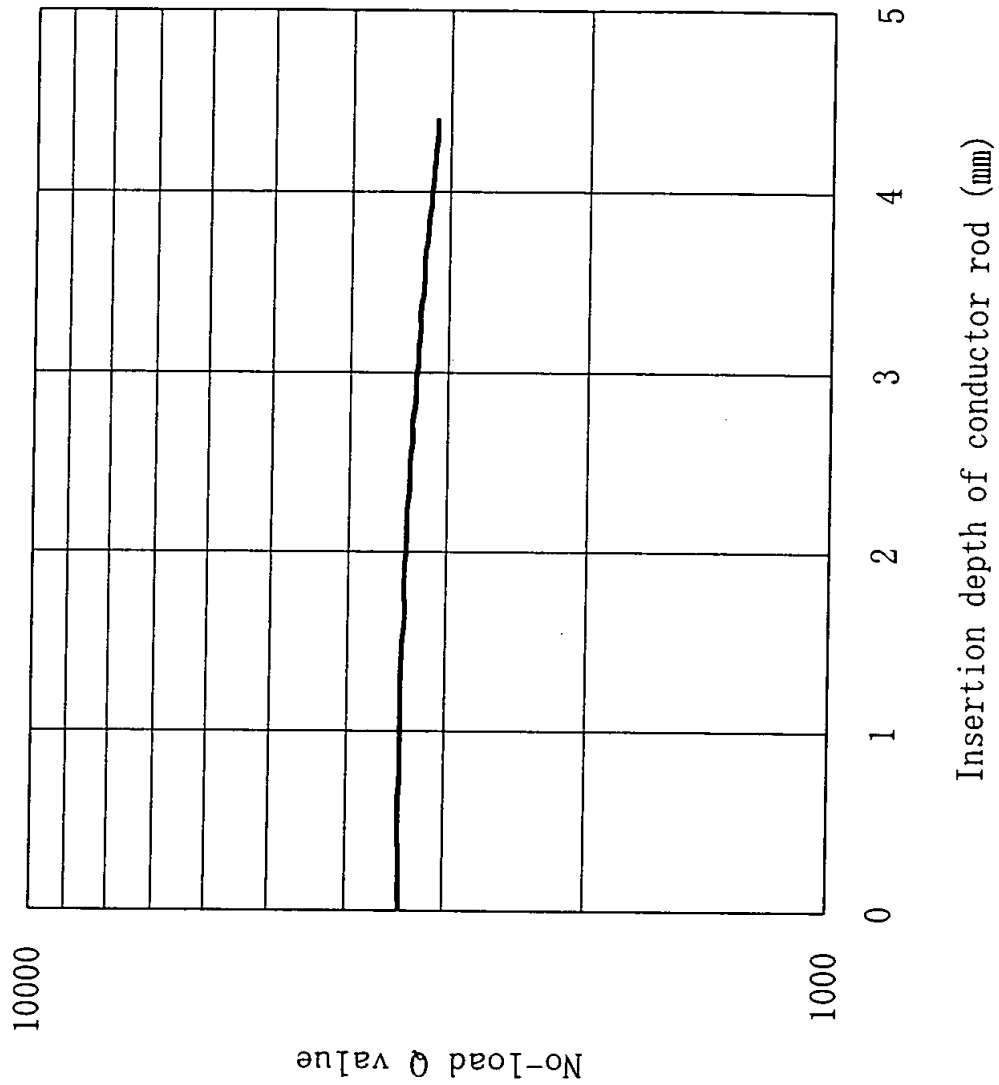


FIG. 11



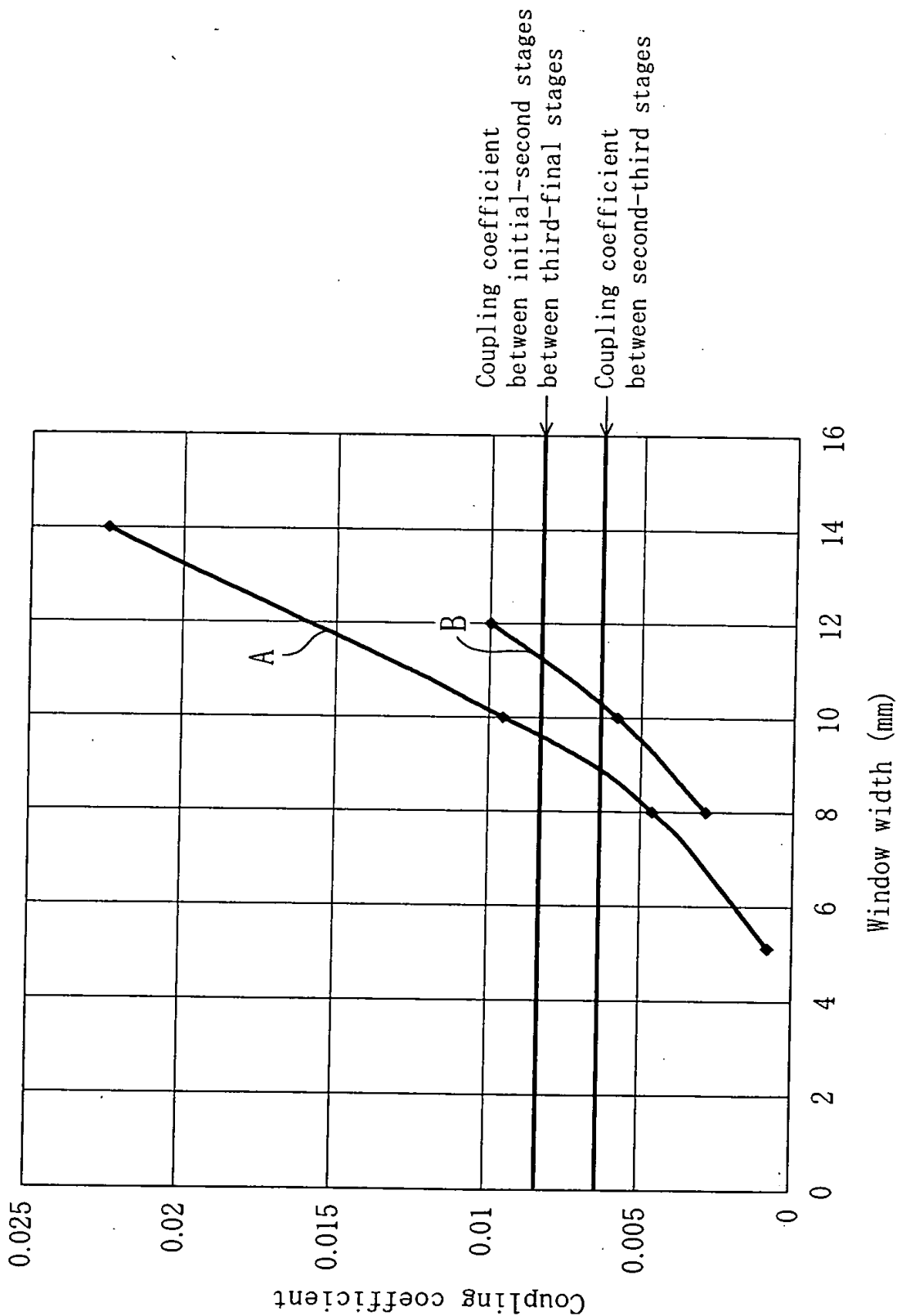
[illegible]



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FIG. 13



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FIG. 14A

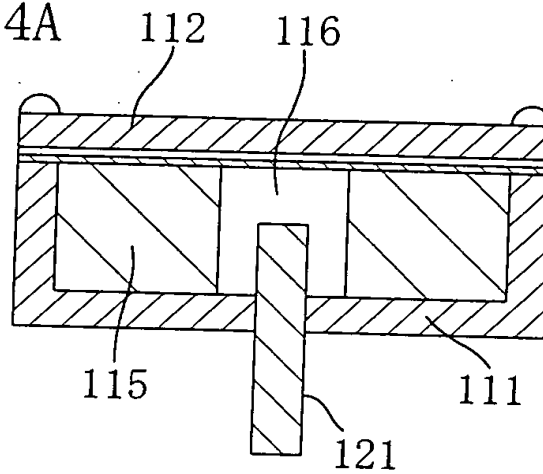


FIG. 14B

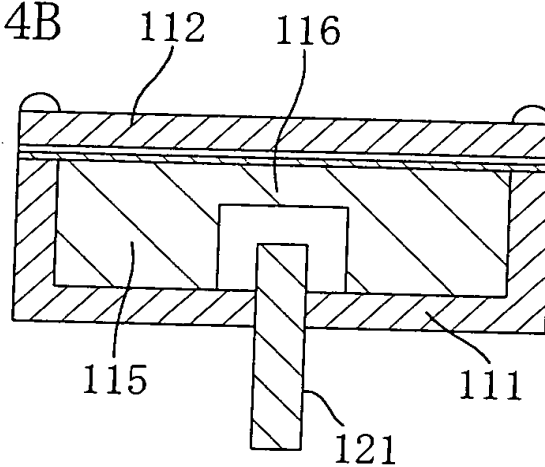
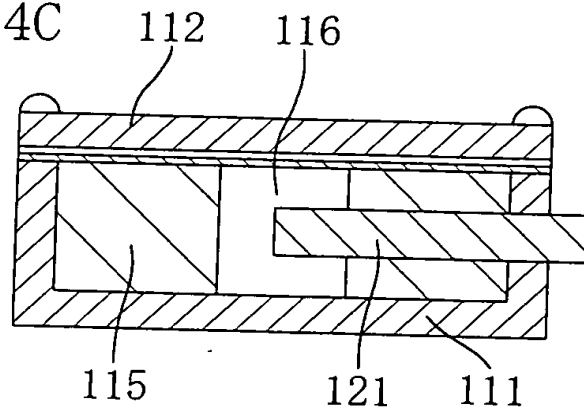


FIG. 14C



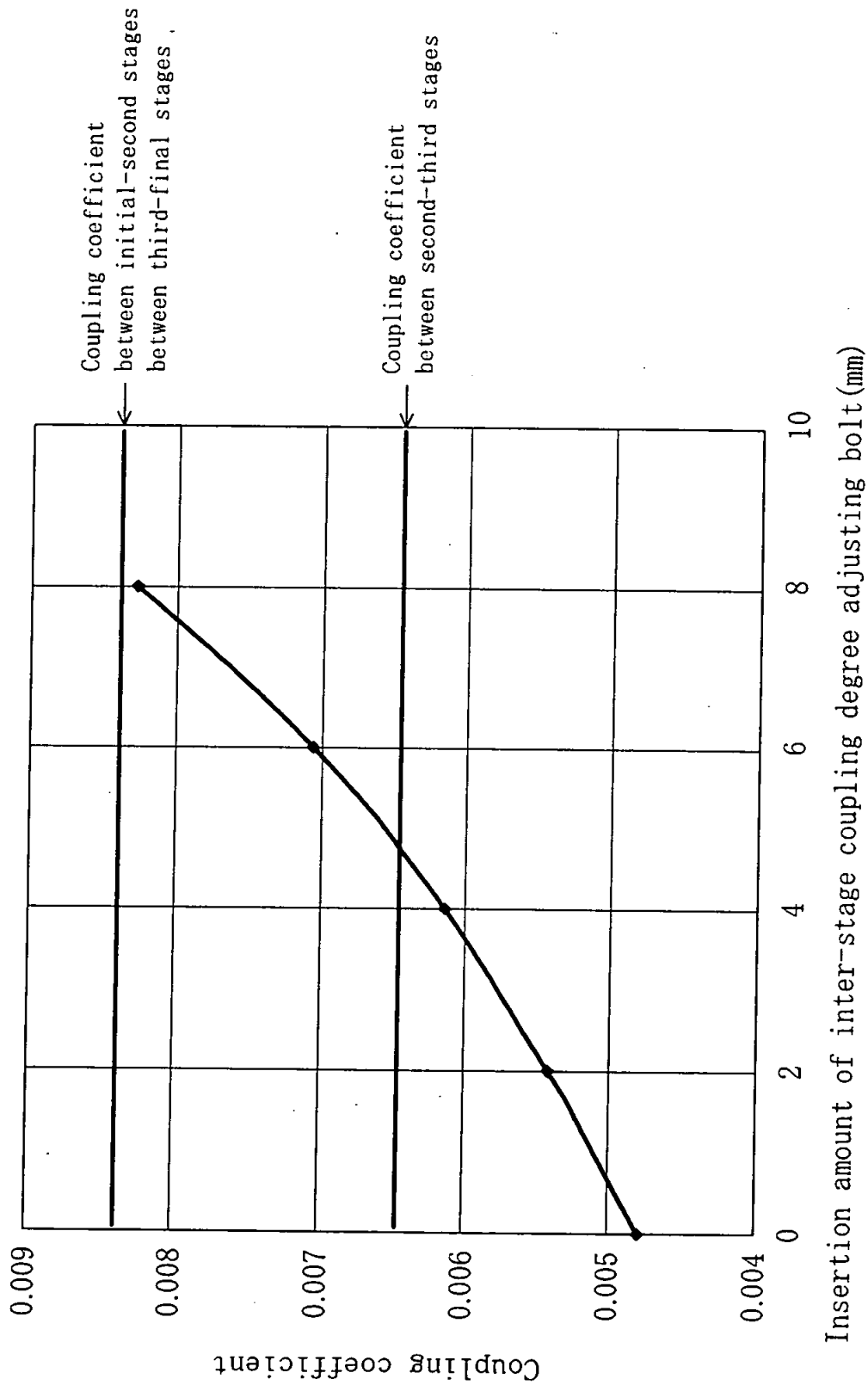
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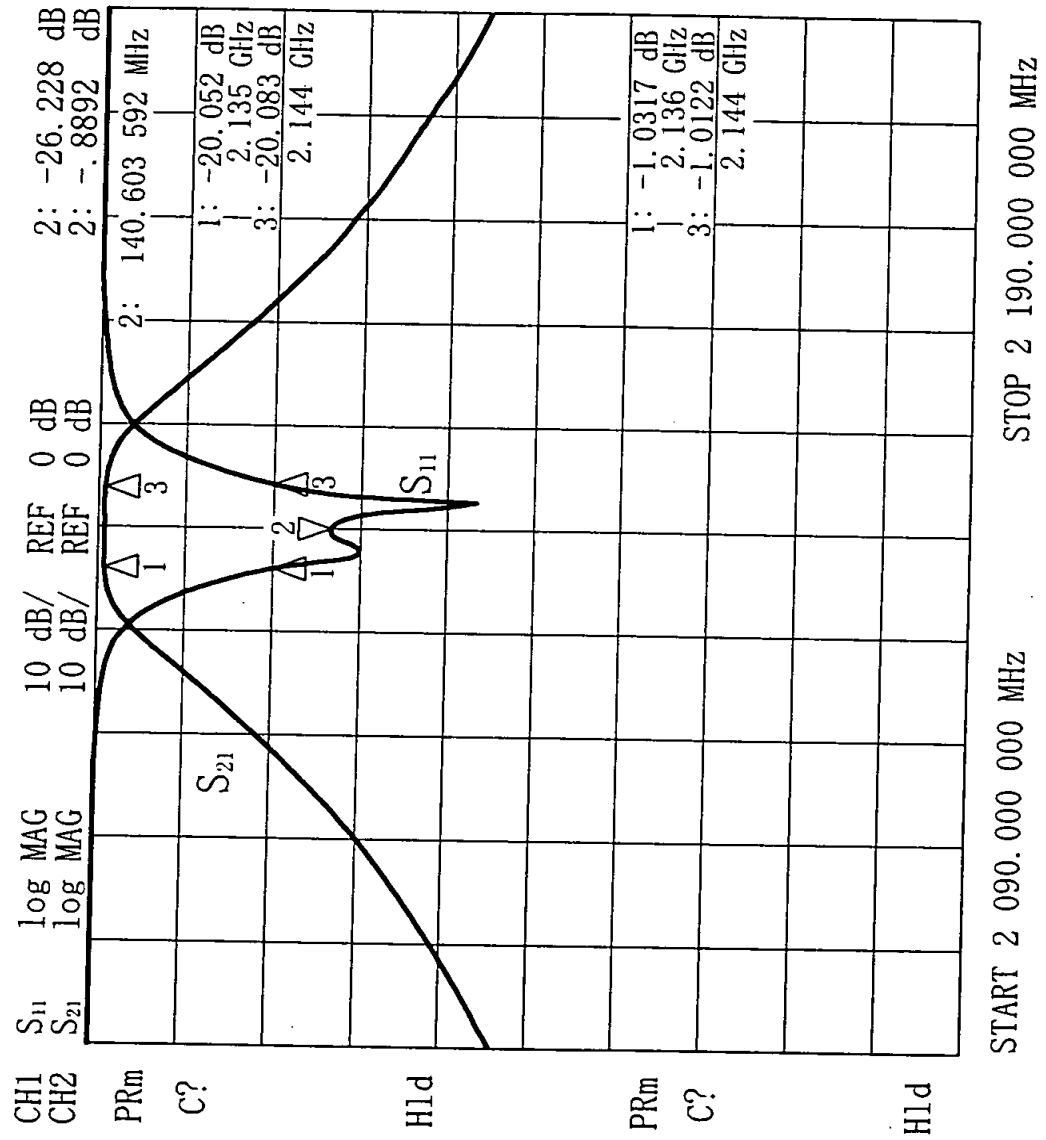
FOH790" SE2F8860

FIG. 15



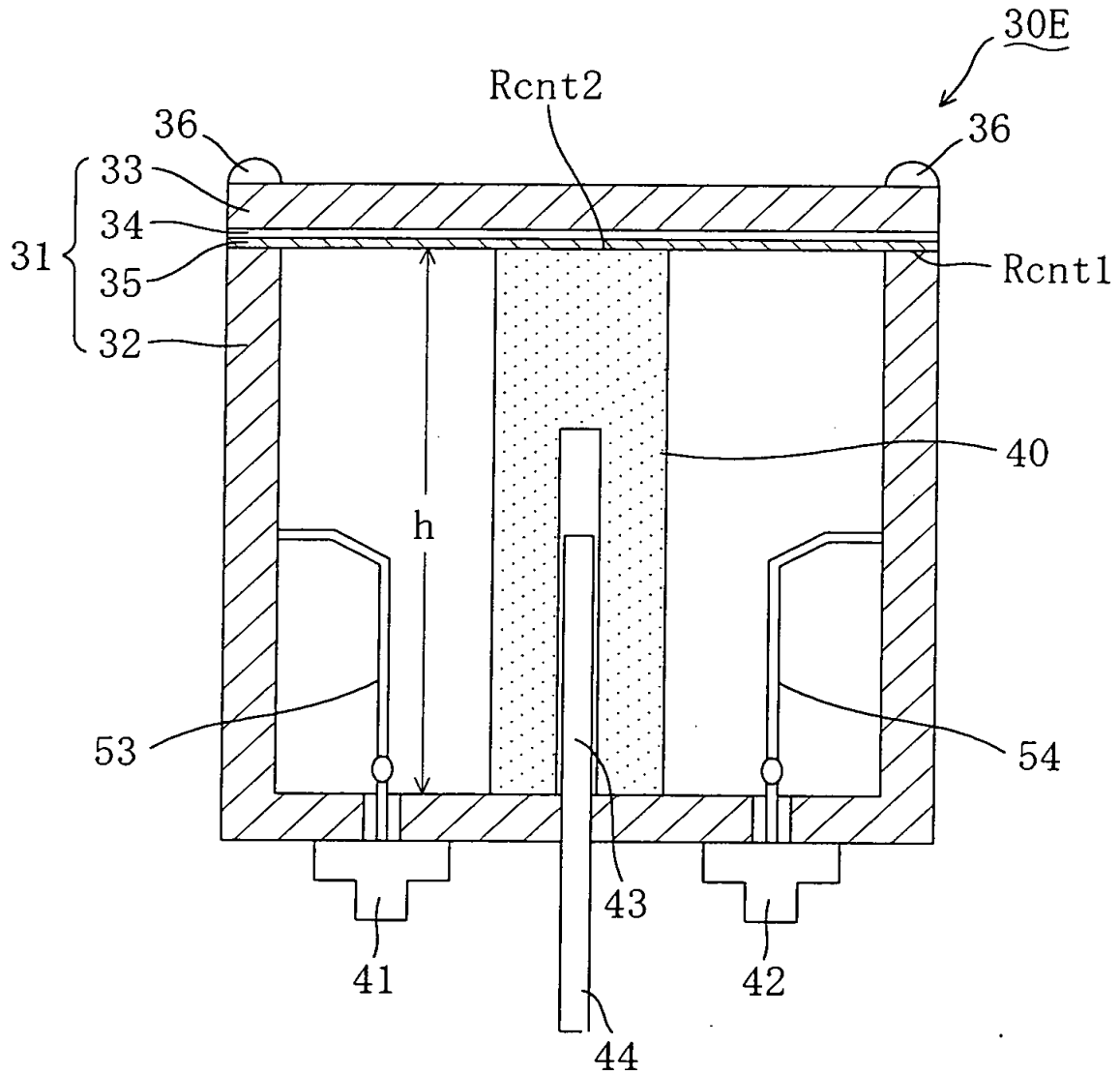
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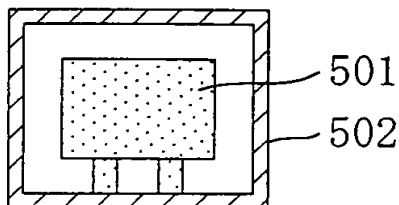


A cross-sectional view of a semiconductor device 30D. The device features a substrate 32 with a top surface 33 and a bottom surface 34. A thin layer 35 is disposed on the top surface 33. A central region 40 is defined by a top surface 36 and a bottom surface 37. This central region 40 is divided into two parts: a first region 51a and a second region 52a. The first region 51a is filled with a material having a dotted pattern, while the second region 52a is empty. The top surface 36 is labeled Rcnt2, and the bottom surface 37 is labeled Rcnt1. The device is mounted on a base 41 via a solder bump 38. A second solder bump 42 is also shown on the bottom surface 34.

FIG. 18



PRIOR ART  
FIG. 19B



PRIOR ART  
FIG. 20

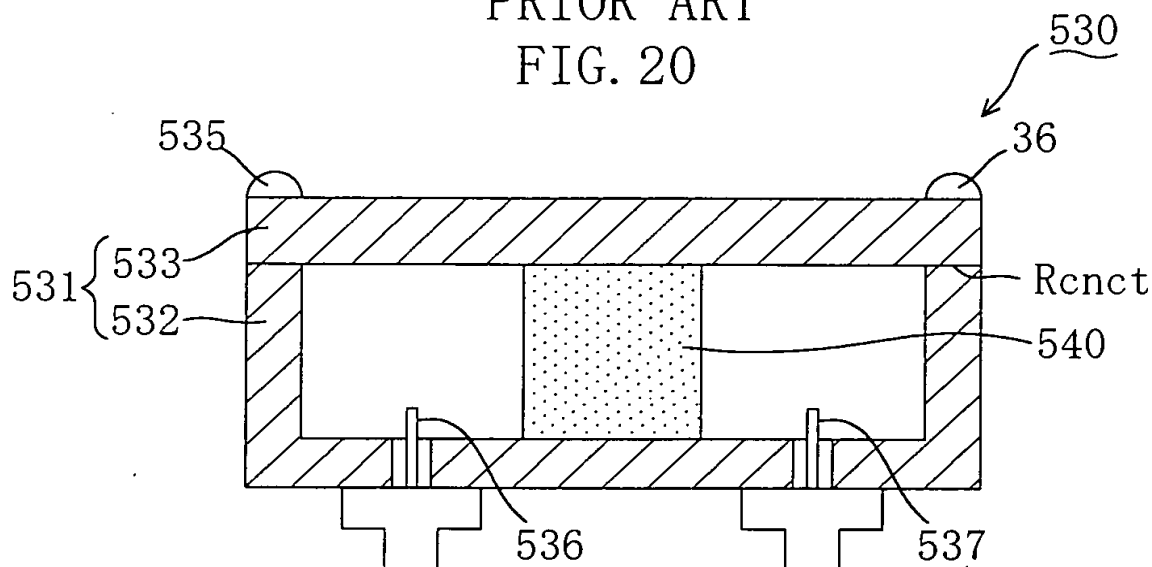


FIG. 21

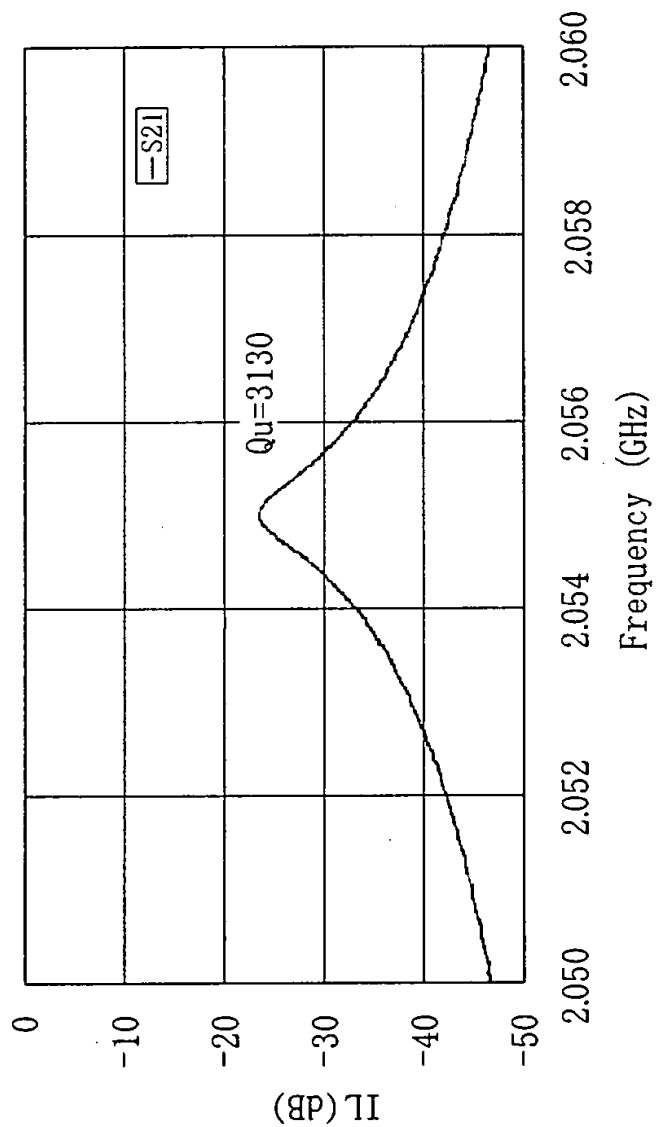


FIG. 21